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New Microlink Structures for CMOS-Compatible Thermopiles

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A highly sensitive infrared (IR) detector requires a large absorption area and a low thermal conductance to maximize the temperature change and signal induced by the incident IR radiation. For the floating membrane of a microsensor, it is difficult to form a large area with suitable front-side etching windows at the same time. A new idea of improving complementary metal-oxide-semiconductor (CMOS) thermopile performance for a floating membrane with a large area is introduced to increase the absorption area, which is constructed by a series of microlinks between each quarter of the membrane. The design and fabrication of the proposed microlink-based thermopiles are realized using 1.2 um CMOS IC technology combined with subsequent anisotropic front-side etching. Four V-groove etching windows were opened by a CMOS process, and then using tetramethylammonium hydroxide (TMAH) etching solution, the silicon substrate was etched along the <100> directions. Finally an Al/n-polysilicon thermopile was embedded in an oxide/nitride membrane. Our large floating membrane has an area of $1300 \times 1300 \ \mu\text{m}^2$ and is 2 μm thick. The floating membrane of the thermopile was formed using four anisotropic etching windows with each quarter of the membrane connected with its nearest membranes. Therefore, the area of the proposed membrane is increased greatly; thus, it absorbs more IR radiation than the conventional design and markedly enhances responsivity. To evaluate the performance of the proposed microlink-based thermopiles, the output voltage frequency response was measured and compared with that of a conventional thermopile. The surface morphology measurement of a proposed thermopile is implemented to evaluate the effect of residual stress and characterize the geometric shape of the membrane practically. The results of etching and the breakage of the microlink-based thermopiles are discussed.

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