Sensors and Materials, Vol. 26, No. 6 (2014) 435–445
MYU Tokyo

S & M 1011

Influence of Pad Surface Asperity on Removal Rate in Chemical Mechanical Polishing of Large-Diameter Silicon Wafer Applied to Substrate of GaN-Based LEDs

Michio Uneda*, Yuki Maeda[1], Kazutaka Shibuya[2], Yoshio Nakamura[2], Daizo Ichikawa[2], Kiyomi Fujii and Ken-ichi Ishikawa

Kanazawa Institute of Technology, 7-1 Ohgigaoka, Nonoichi, Ishikawa 921-8501, Japan
[1]Graduate School of Kanazawa Institute of Technology,
7-1 Ohgigaoka, Nonoichi, Ishikawa 921-8501, Japan
[2]Fujikoshi Machinery Corp., 1650 Kiyono, Matsushiro-machi, Nagano 381-1233, Japan

(Received December 26, 2013; accepted April 17, 2014)

Key words: silicon wafer, GaN growth substrate, polishing, pad surface asperity, contact image analysis, removal rate, multiple correlation analysis

Currently, large-diameter silicon (Si) wafers have been applied to the substrate of GaN-based light-emitting diodes (LEDs) for realizing low carbon societies at a low cost. In the Si polishing process, the removal rate is strongly dependent on the pad surface asperity. We have developed a quantitative evaluation method based on contact image analysis using an image rotation prism. In this paper, we discuss the influences of pad surface asperity on removal rate for Si wafers determined by various polishing tests. The results indicated a high removal rate in the following case: number of contact points, 30/mm^2; contact ratio, 0.8%; spacing of contact points, 450 μm; and spatial fast Fourier transform (FFT) results, 100 μm. Furthermore, the removal rate can be precisely estimated using four evaluation parameters by multiple correlation analysis.

*Corresponding author: e-mail: uneda@neptune.kanazawa-it.ac.jp